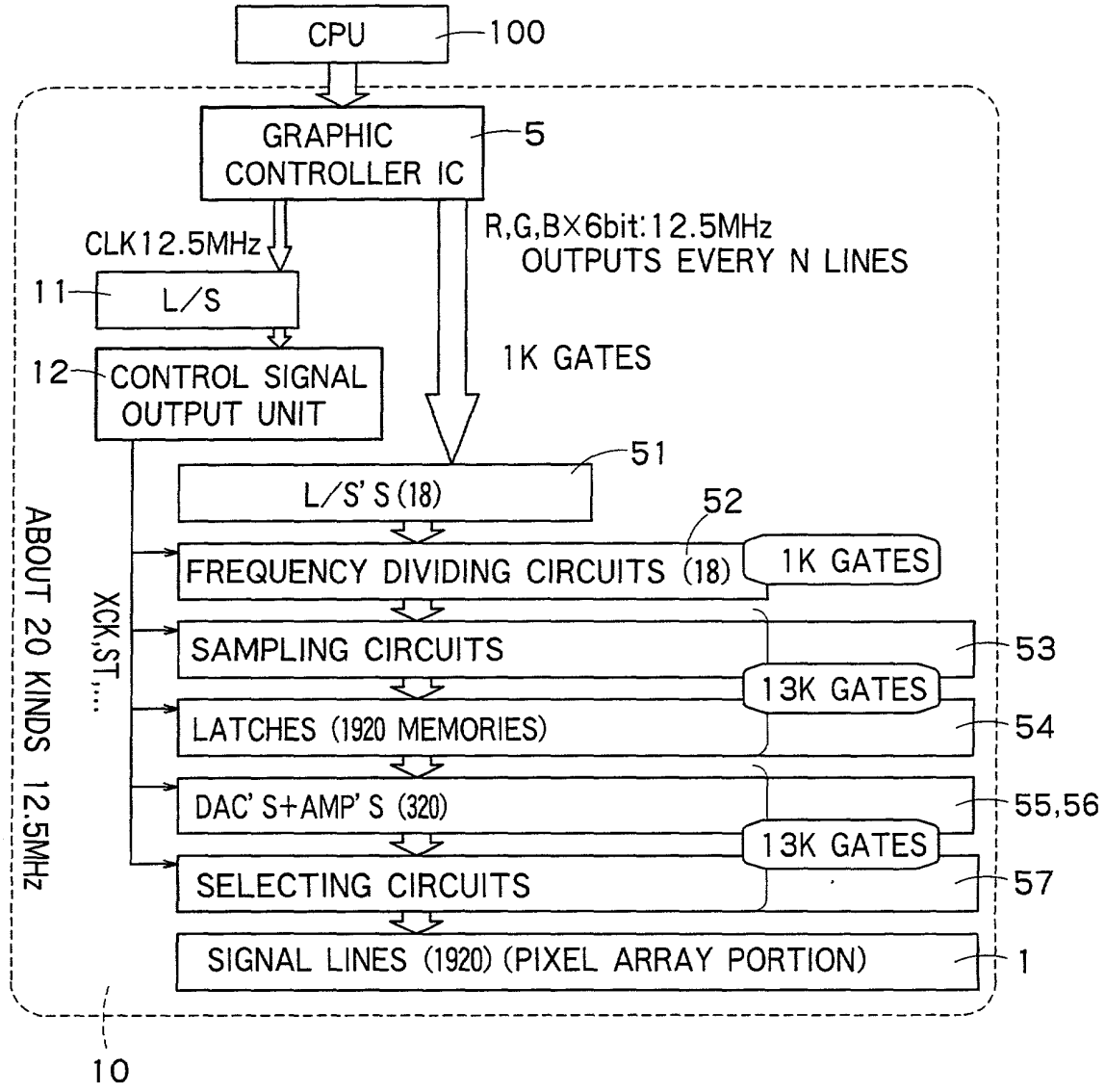
CPU
100
GRAPHIC CONTROLLER IC
5
CLK12.5MHz
R,G,B×6bit:12.5MHz
OUTPUTS EVERY N LINES
11
L/S
12
CONTROL SIGNAL OUTPUT UNIT
1K GATES
51
L/S'S(18)
52
FREQUENCY DIVIDING CIRCUITS (18)
1K GATES
SAMPLING CIRCUITS
53
13K GATES
LATCHES (1920 MEMORIES)
54
DAC'S+AMP'S (320)
55,56
13K GATES
SELECTING CIRCUITS
57
SIGNAL LINES (1920) (PIXEL ARRAY PORTION)
1
ABOUT 20 KINDS 12.5MHz
XCK,ST,...
10

FIG. 1

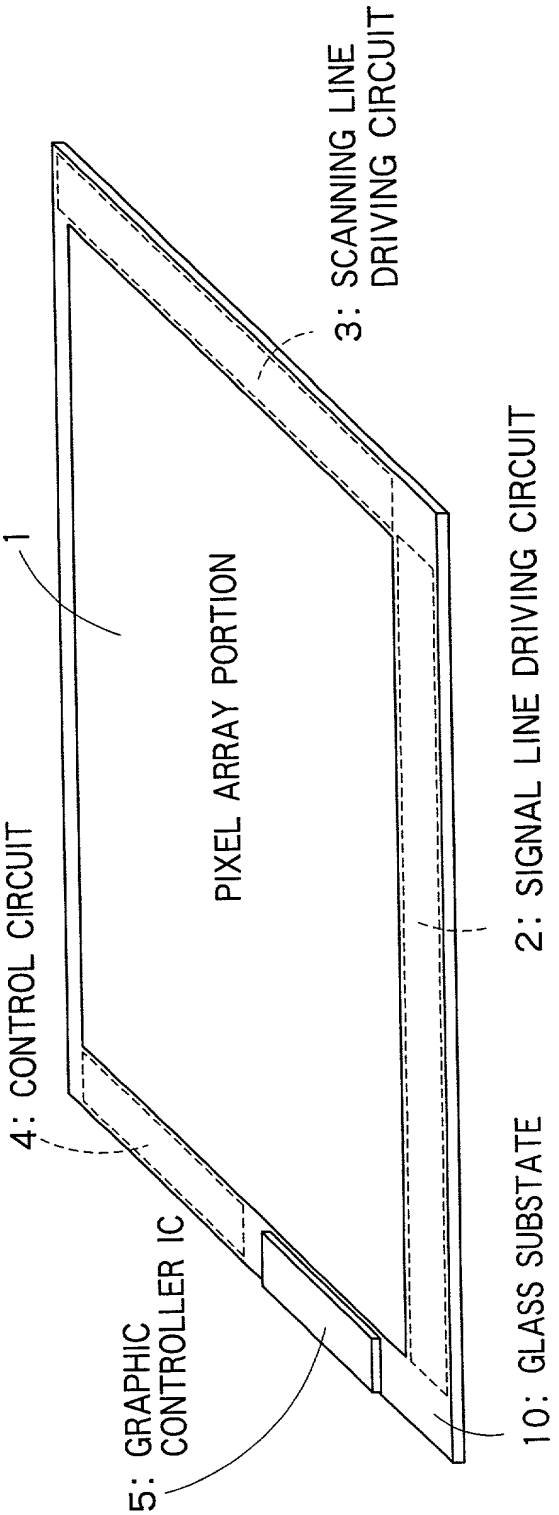
3: SCANNING LINE DRIVING CIRCUIT
1
PIXEL ARRAY PORTION
2: SIGNAL LINE DRIVING CIRCUIT
4: CONTROL CIRCUIT
5: GRAPHIC CONTROLLER IC
10: GLASS SUBSTATE

FIG. 2

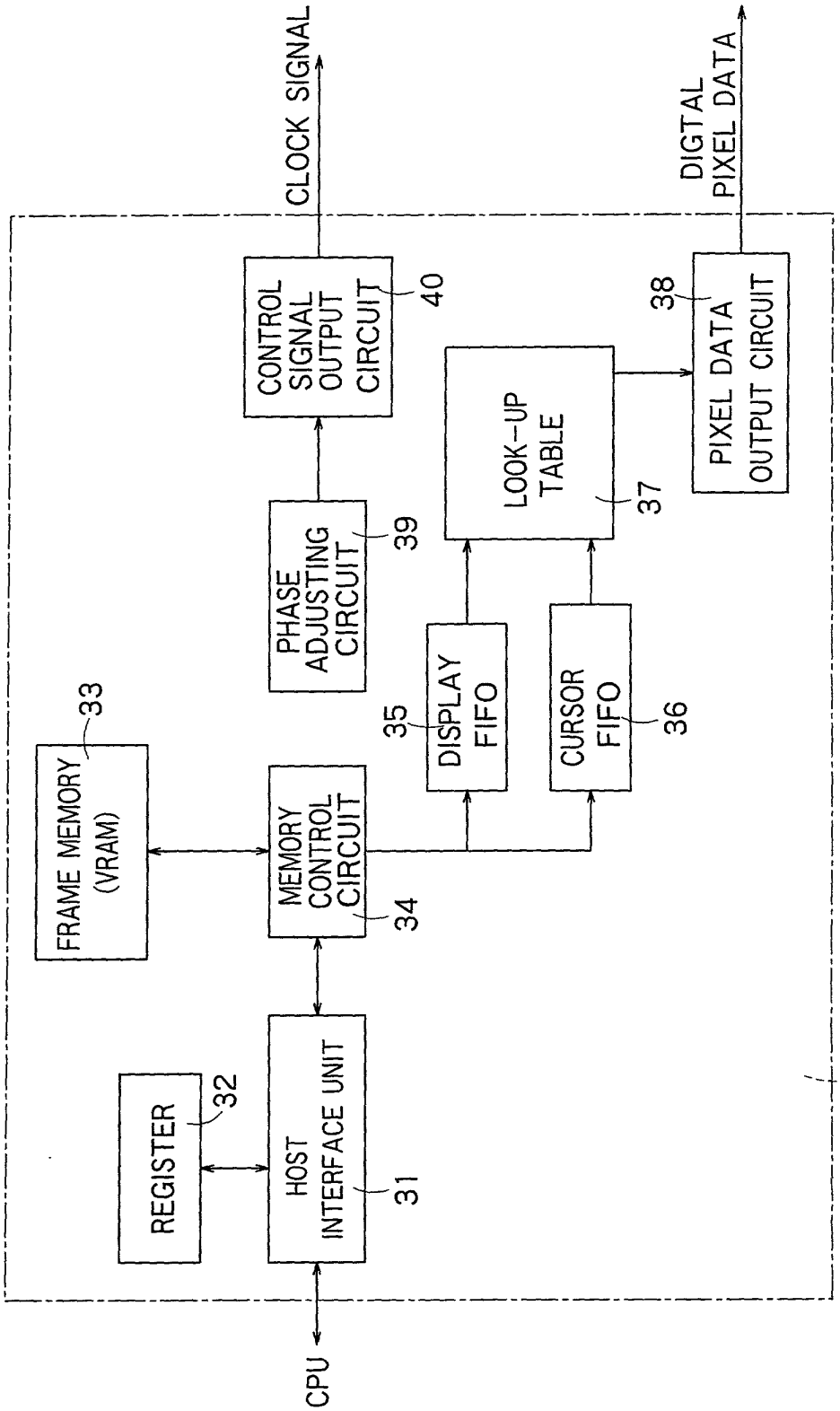
CLOCK SIGNAL
DIGTAL PIXEL DATA
CONTROL SIGNAL OUTPUT CIRCUIT
40
38
PIXEL DATA OUTPUT CIRCUIT
LOOK-UP TABLE
37
PHASE ADJUSTING CIRCUIT
39
DISPLAY FIFO
35
CURSOR FIFO
36
FRAME MEMORY (VRAM)
33
MEMORY CONTROL CIRCUIT
34
REGISTER
32
HOST INTERFACE UNIT
31
CPU
5: GRAPHIC CONTROLLER IC

FIG. 3

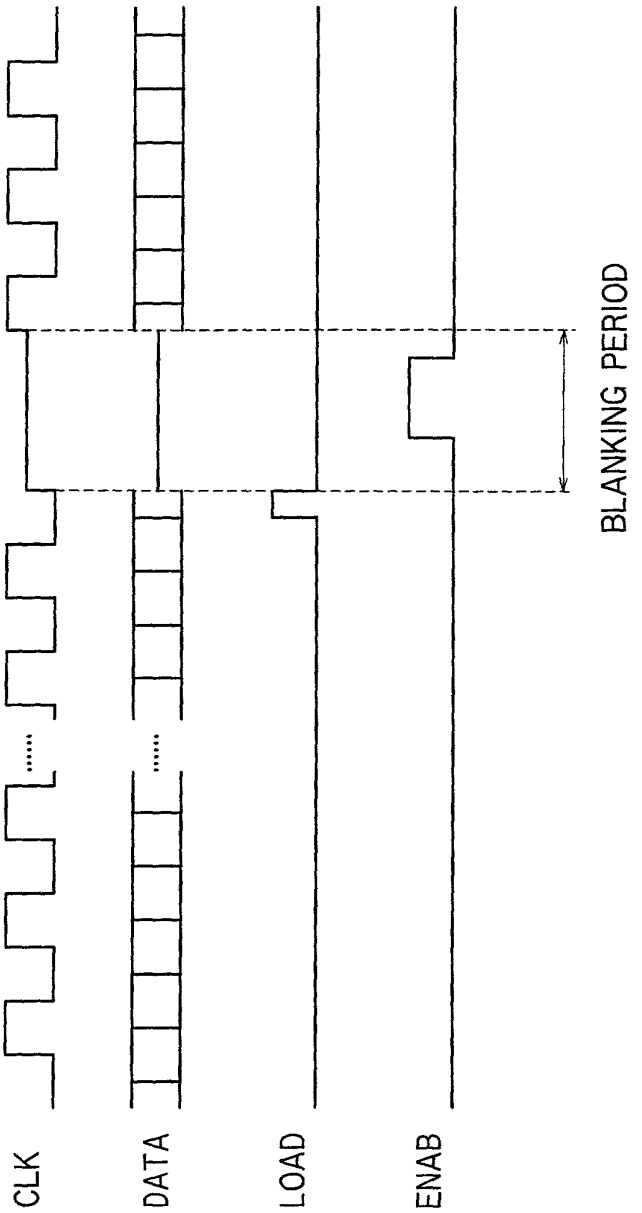

FIG. 4

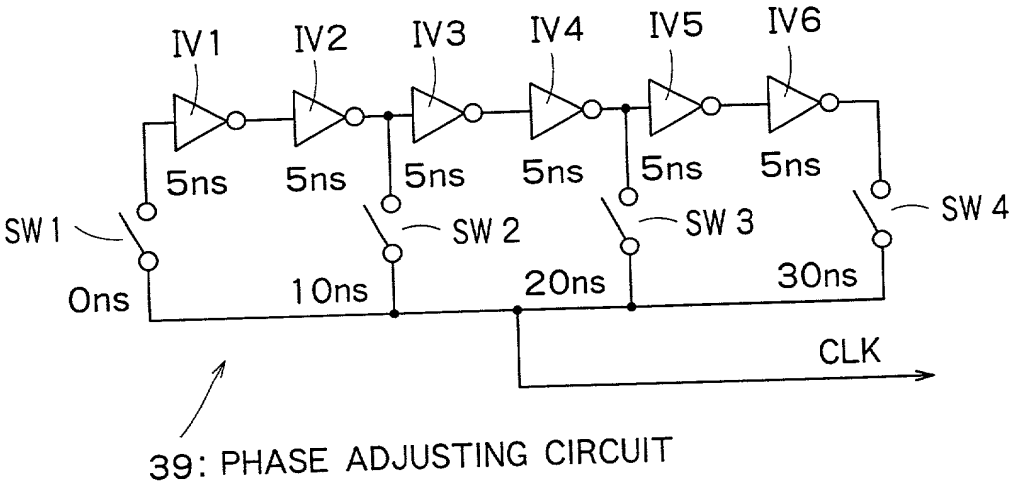
IV1
IV2
IV3
IV4
IV5
IV6
5ns
5ns
5ns
5ns
5ns
5ns
SW 1
SW 2
SW 3
SW 4
0ns
10ns
20ns
30ns
CLK
39: PHASE ADJUSTING CIRCUIT

FIG. 5

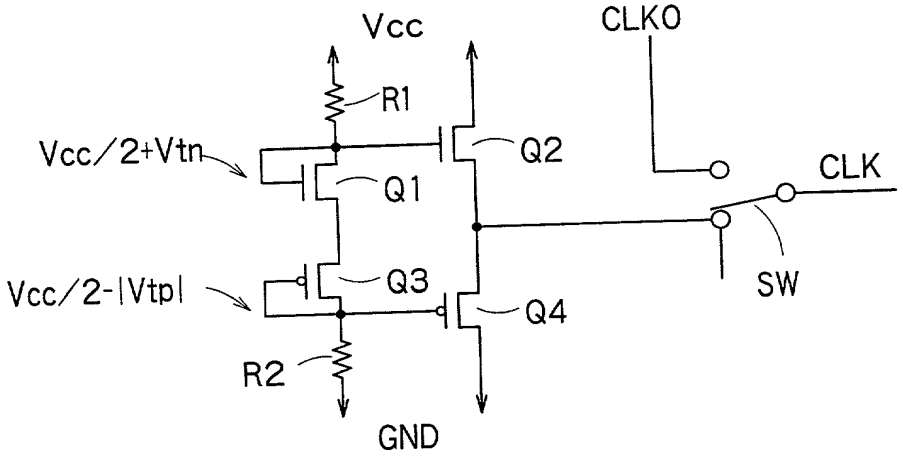
Vcc
CLK0
R1
Vcc/2+Vtn
Q2
Q1
CLK
Vcc/2-|Vtp|
Q3
Q4
SW
R2
GND

FIG. 6

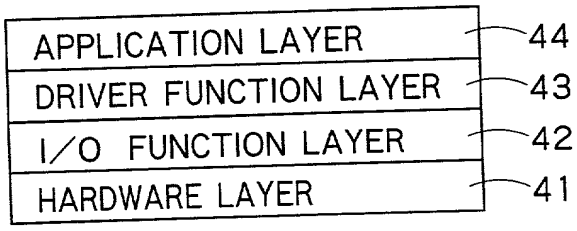
APPLICATION LAYER
44
DRIVER FUNCTION LAYER
43
I/O FUNCTION LAYER
42
HARDWARE LAYER
41

FIG. 7

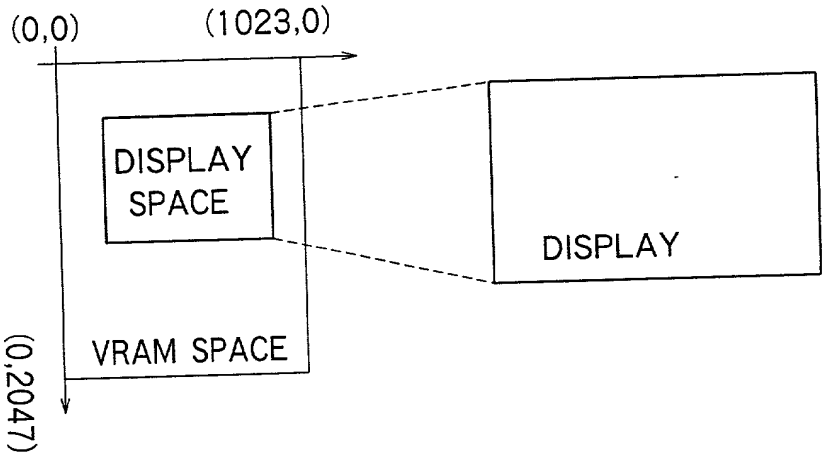
(0,0)
(1023,0)
DISPLAY SPACE
DISPLAY
VRAM SPACE
(0,2047)

FIG. 8

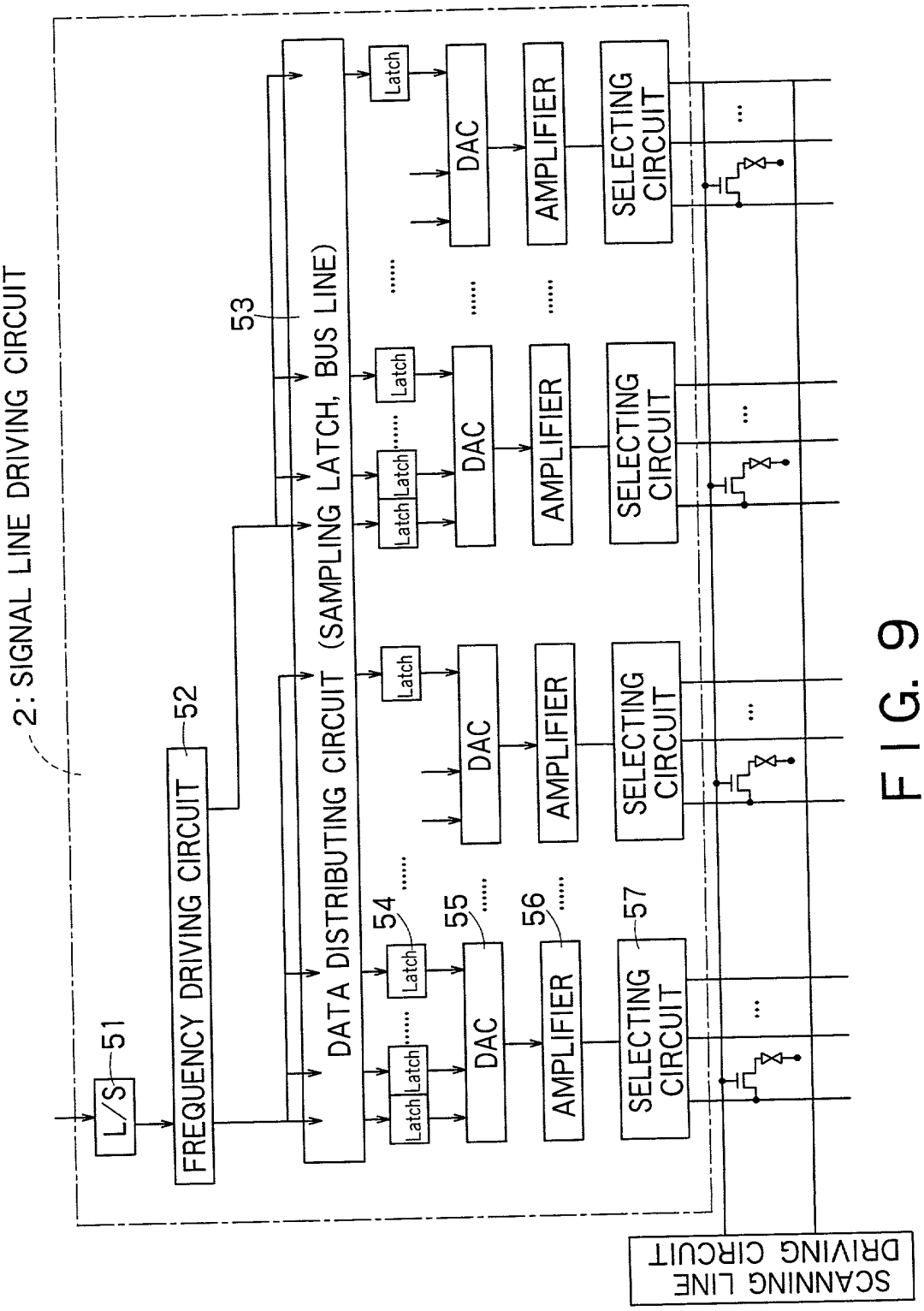
2: SIGNAL LINE DRIVING CIRCUIT
L/S
51
FREQUENCY DRIVING CIRCUIT
52
DATA DISTRIBUTING CIRCUIT (SAMPLING LATCH, BUS LINE)
53
Latch
54
DAC
55
AMPLIFIER
56
SELECTING CIRCUIT
57
SCANNING LINE DRIVING CIRCUIT

FIG. 9

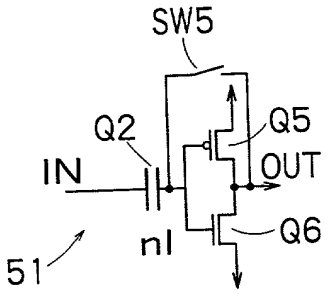

FIG. 10

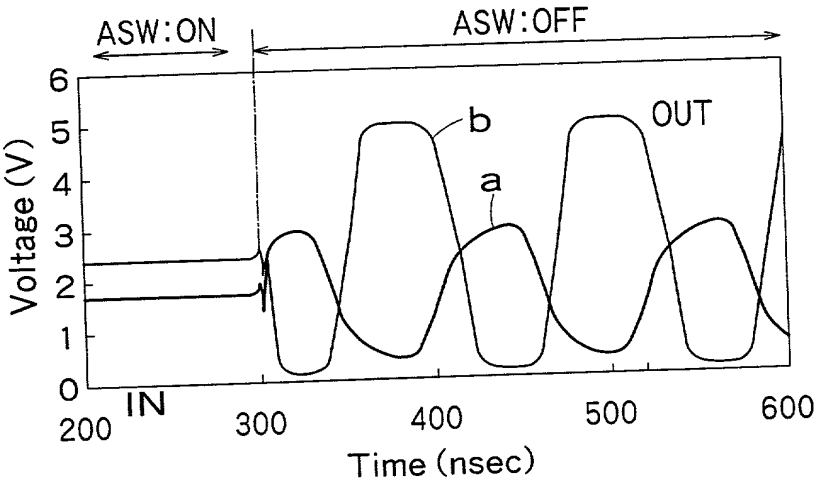

FIG. 11

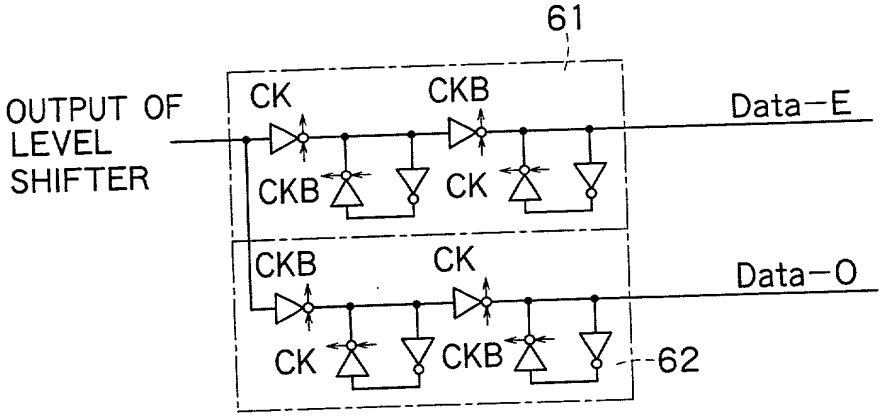

FIG. 12

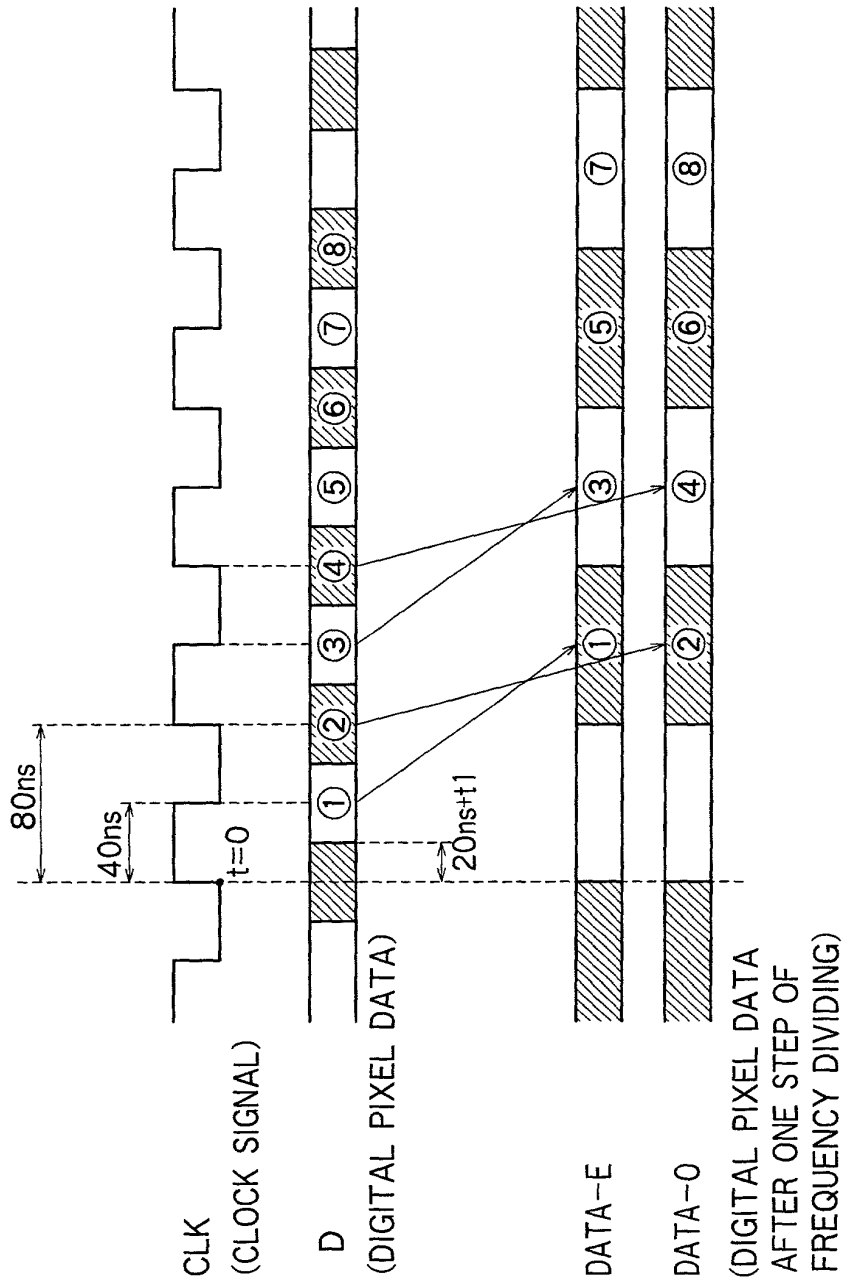
80ns
40ns
t=0
20ns+t1
CLK
(CLOCK SIGNAL)
D
(DIGITAL PIXEL DATA)
DATA-E
DATA-O
(DIGITAL PIXEL DATA
AFTER ONE STEP OF
FREQUENCY DIVIDING)

FIG. 13

10 / 30

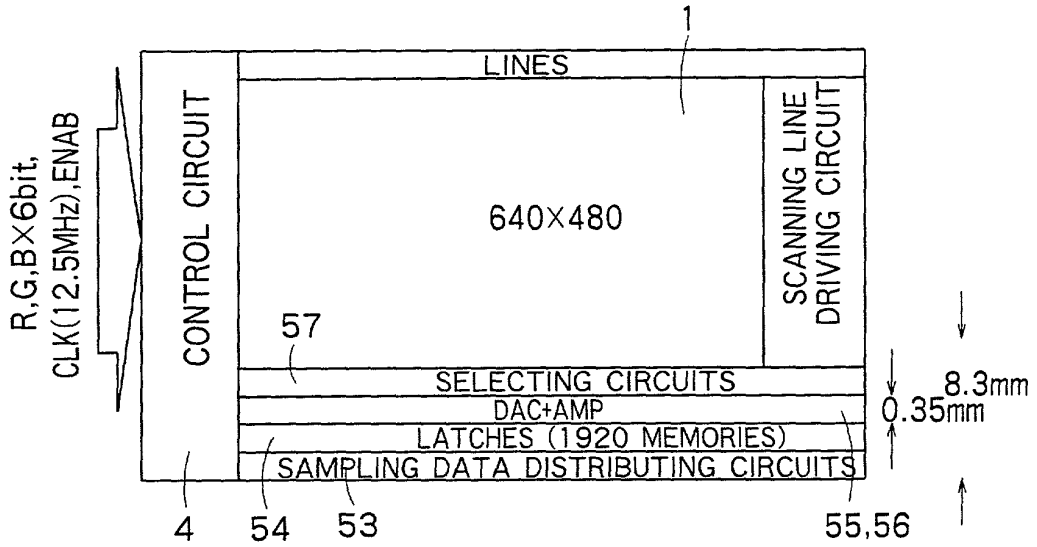

FIG. 14

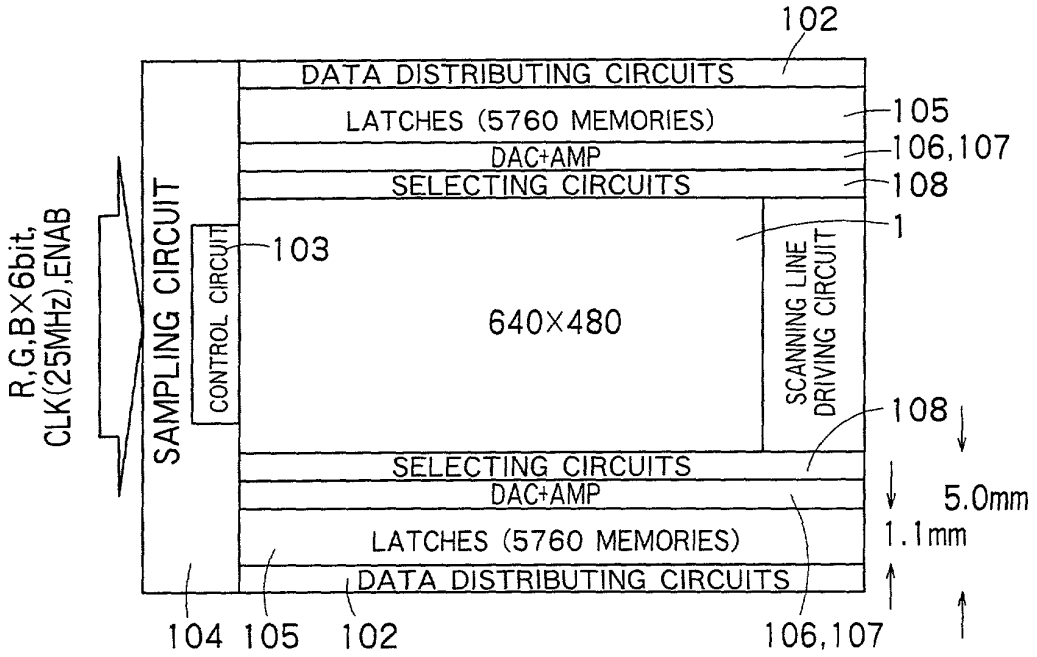

FIG. 15

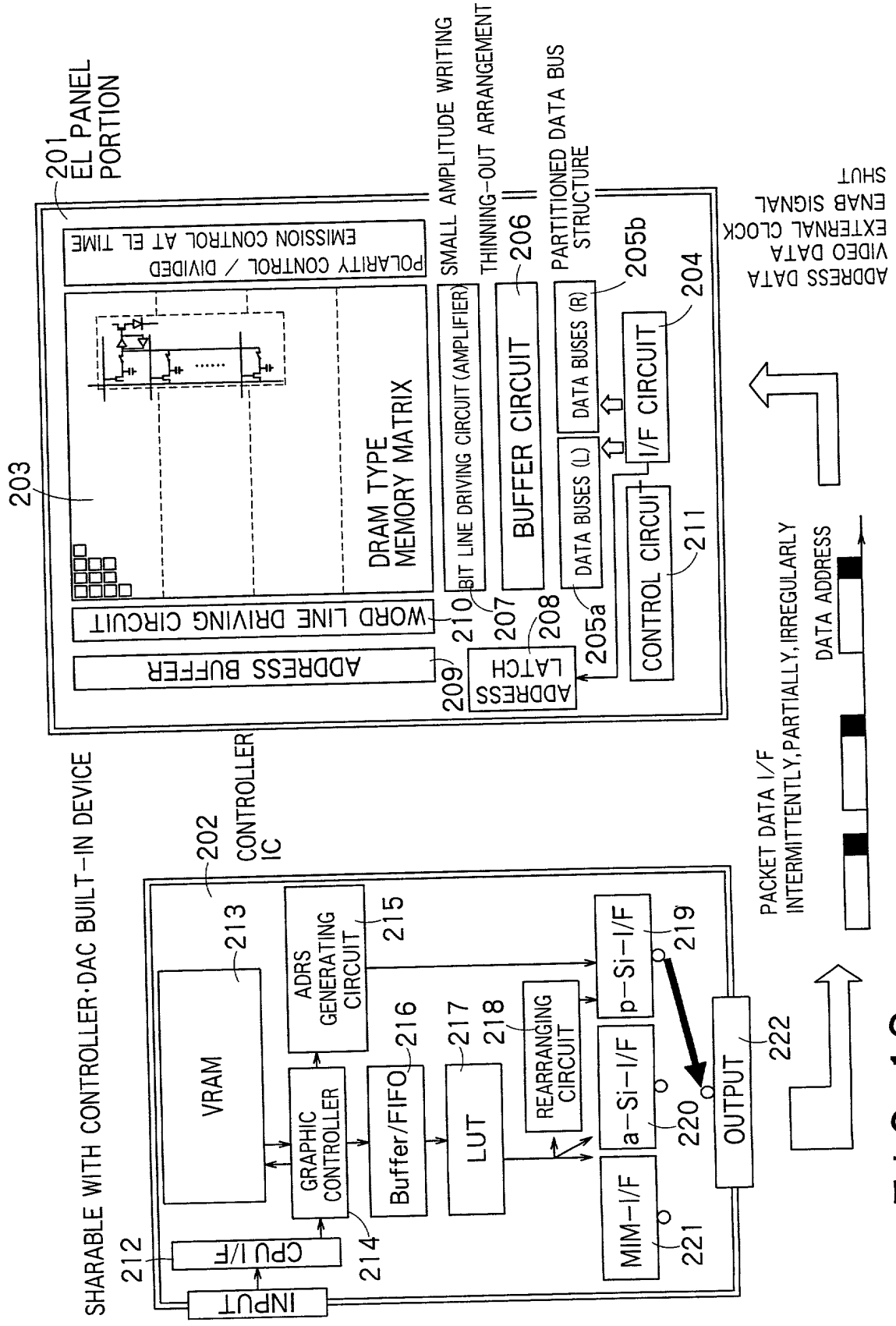
201
EL PANEL PORTION
POLARITY CONTROL / DIVIDED EMISSION CONTROL AT EL TIME
203
DRAM TYPE MEMORY MATRIX
SMALL AMPLITUDE WRITING
THINNING-OUT ARRANGEMENT
PARTITIONED DATA BUS STRUCTURE
206
BUFFER CIRCUIT
BIT LINE DRIVING CIRCUIT (AMPLIFIER)
WORD LINE DRIVING CIRCUIT
ADDRESS BUFFER
210
207
208
209
ADDRESS LATCH
205a
DATA BUSES (L)
DATA BUSES (R)
205b
I/F CIRCUIT
204
CONTROL CIRCUIT
211
ADDRESS DATA
VIDEO DATA
EXTERNAL CLOCK
ENAB SIGNAL
SHUT
PACKET DATA I/F
INTERMITTENTLY, PARTIALLY, IRREGULARLY
DATA ADDRESS
SHARABLE WITH CONTROLLER·DAC BUILT-IN DEVICE
202
CONTROLLER IC
213
VRAM
ADRS GENERATING CIRCUIT
215
GRAPHIC CONTROLLER
216
Buffer/FIFO
217
LUT
218
REARRANGING CIRCUIT
p-Si-I/F
219
a-Si-I/F
220
MIM-I/F
221
OUTPUT
222
CPU I/F
212
214
INPUT

FIG. 16

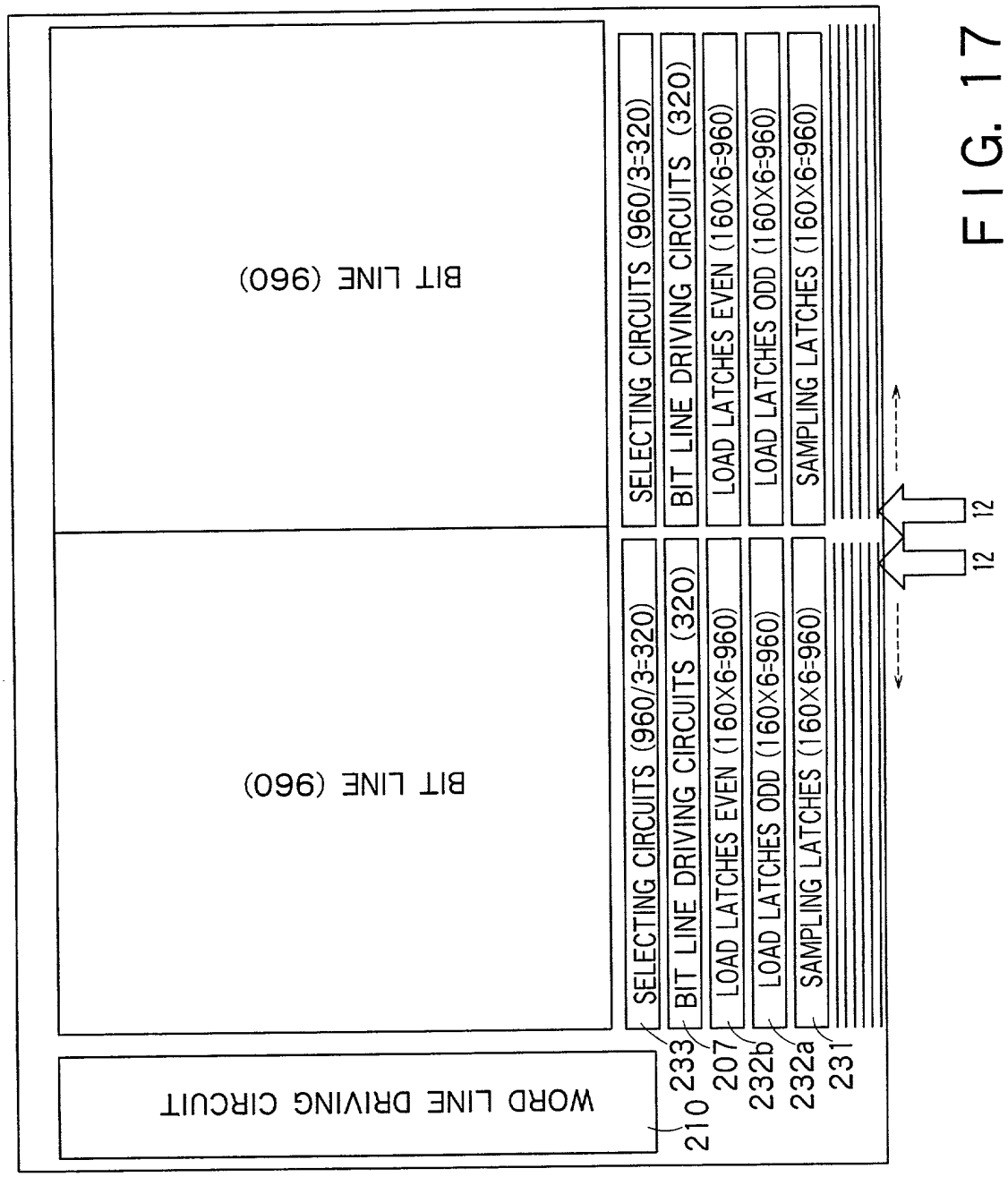
BIT LINE (960)
BIT LINE (960)
WORD LINE DRIVING CIRCUIT
210
SELECTING CIRCUITS (960/3=320)
BIT LINE DRIVING CIRCUITS (320)
LOAD LATCHES EVEN (160X6=960)
LOAD LATCHES ODD (160X6=960)
SAMPLING LATCHES (160X6=960)
233
207
232b
232a
231
12
12
12

FIG. 17

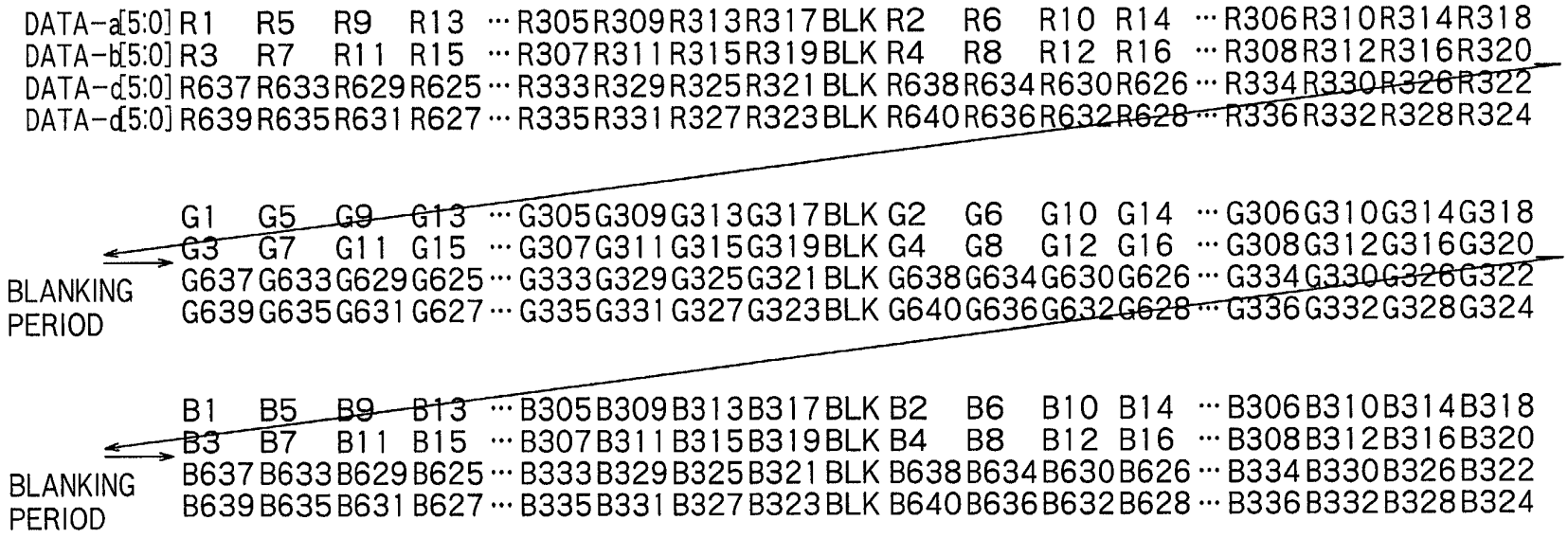

FIG. 18

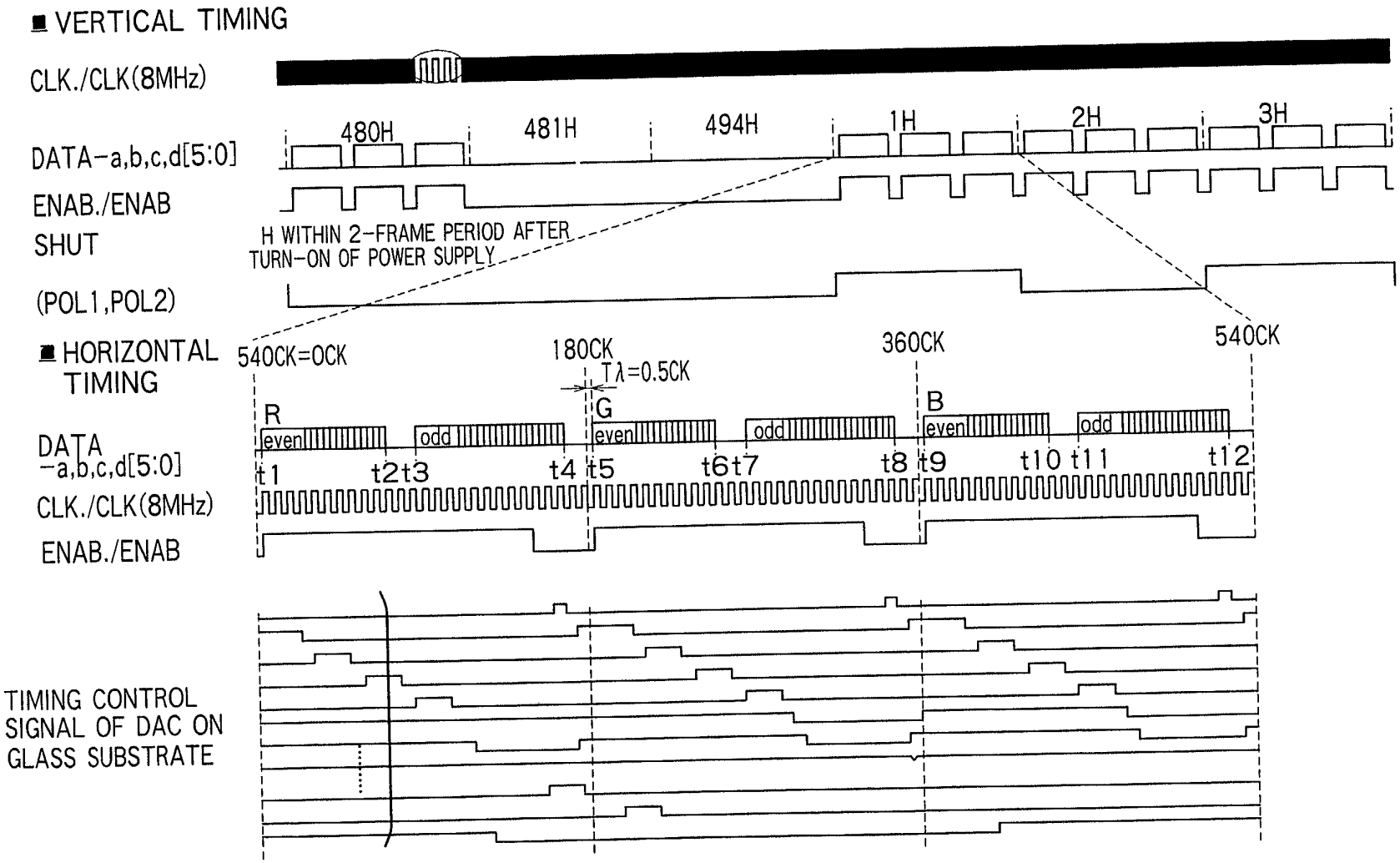

FIG. 19

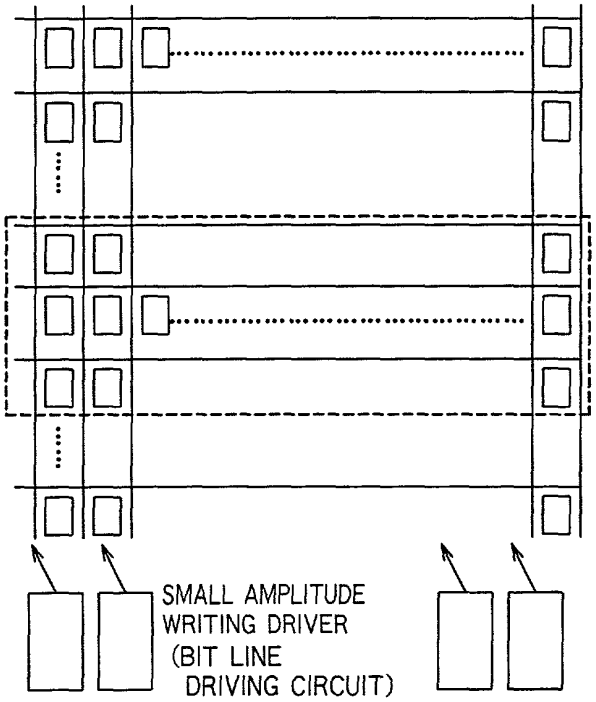

FIG. 20A

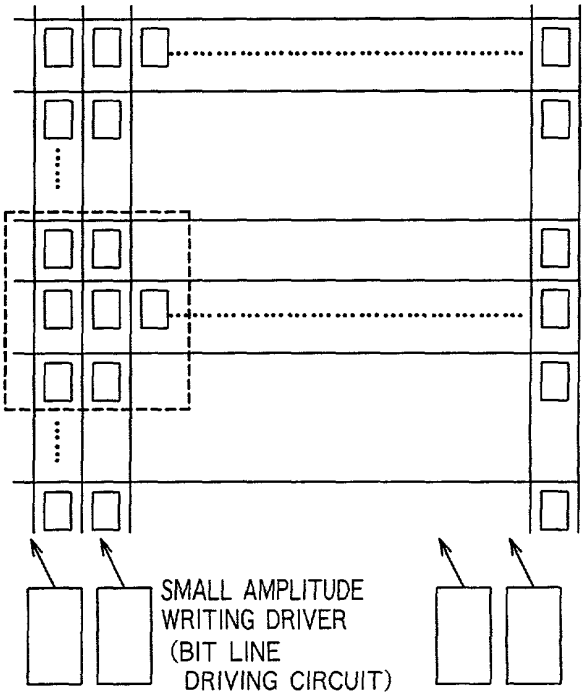

FIG. 20B

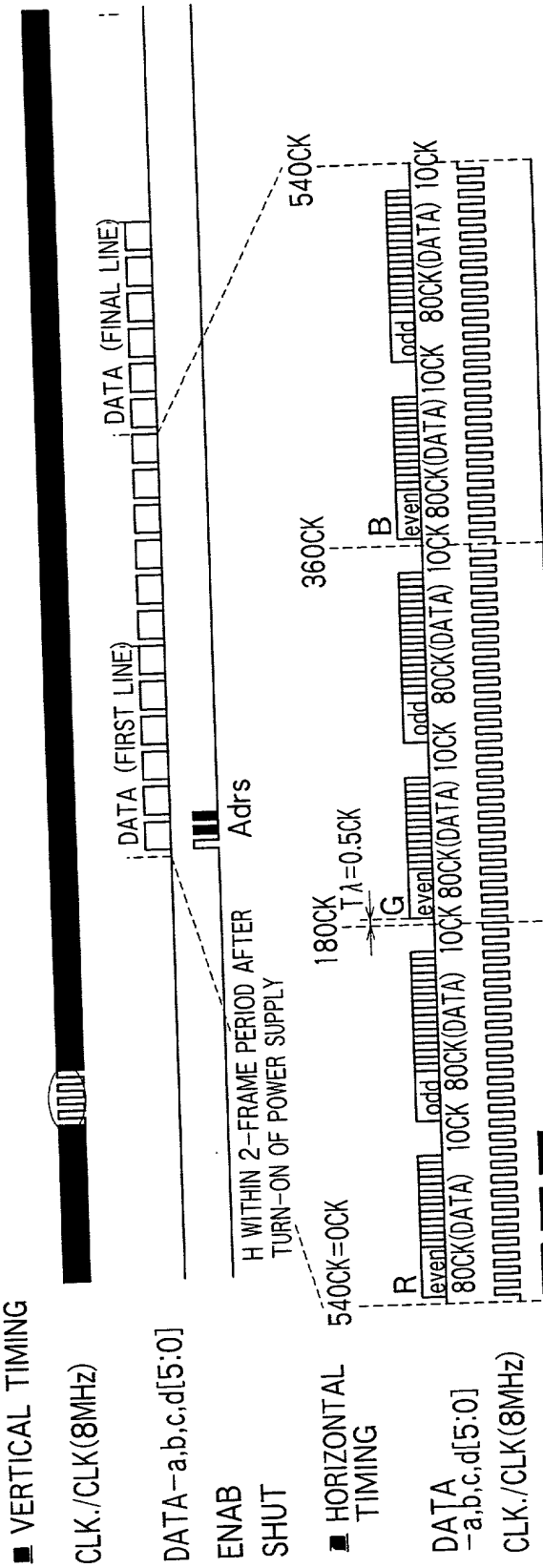
■ VERTICAL TIMING
CLK./CLK(8MHz)
DATA-a,b,c,d[5:0]
ENAB
SHUT
DATA (FIRST LINE)
DATA (FINAL LINE)
Adrs
H WITHIN 2-FRAME PERIOD AFTER TURN-ON OF POWER SUPPLY
540CK
360CK
180CK
Tλ=0.5CK
■ HORIZONTAL TIMING
540CK=0CK
R
G
B
DATA -a,b,c,d[5:0]
CLK./CLK(8MHz)
EMAB./EMAB
leven
lodd
80CK(DATA)
10CK
Adrs

FIG. 21

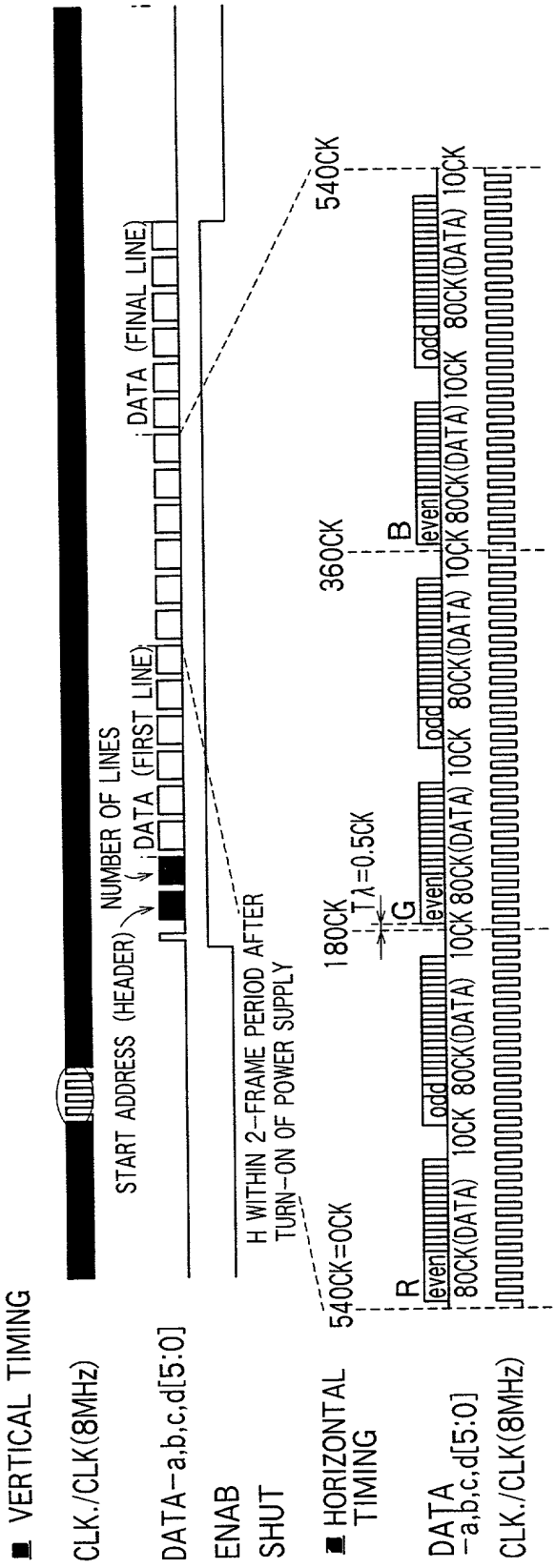
■ VERTICAL TIMING
CLK./CLK(8MHz)
START ADDRESS (HEADER)
NUMBER OF LINES
DATA (FIRST LINE)
DATA (FINAL LINE)
DATA-a,b,c,d[5:0]
ENAB
H WITHIN 2-FRAME PERIOD AFTER TURN-ON OF POWER SUPPLY
SHUT
■ HORIZONTAL TIMING
540CK=0CK
180CK
360CK
540CK
Tλ=0.5CK
R
G
B
even
odd
80CK(DATA) 10CK 80CK(DATA) 10CK 80CK(DATA) 10CK 80CK(DATA) 10CK
DATA -a,b,c,d[5:0]
CLK./CLK(8MHz)

FIG. 22

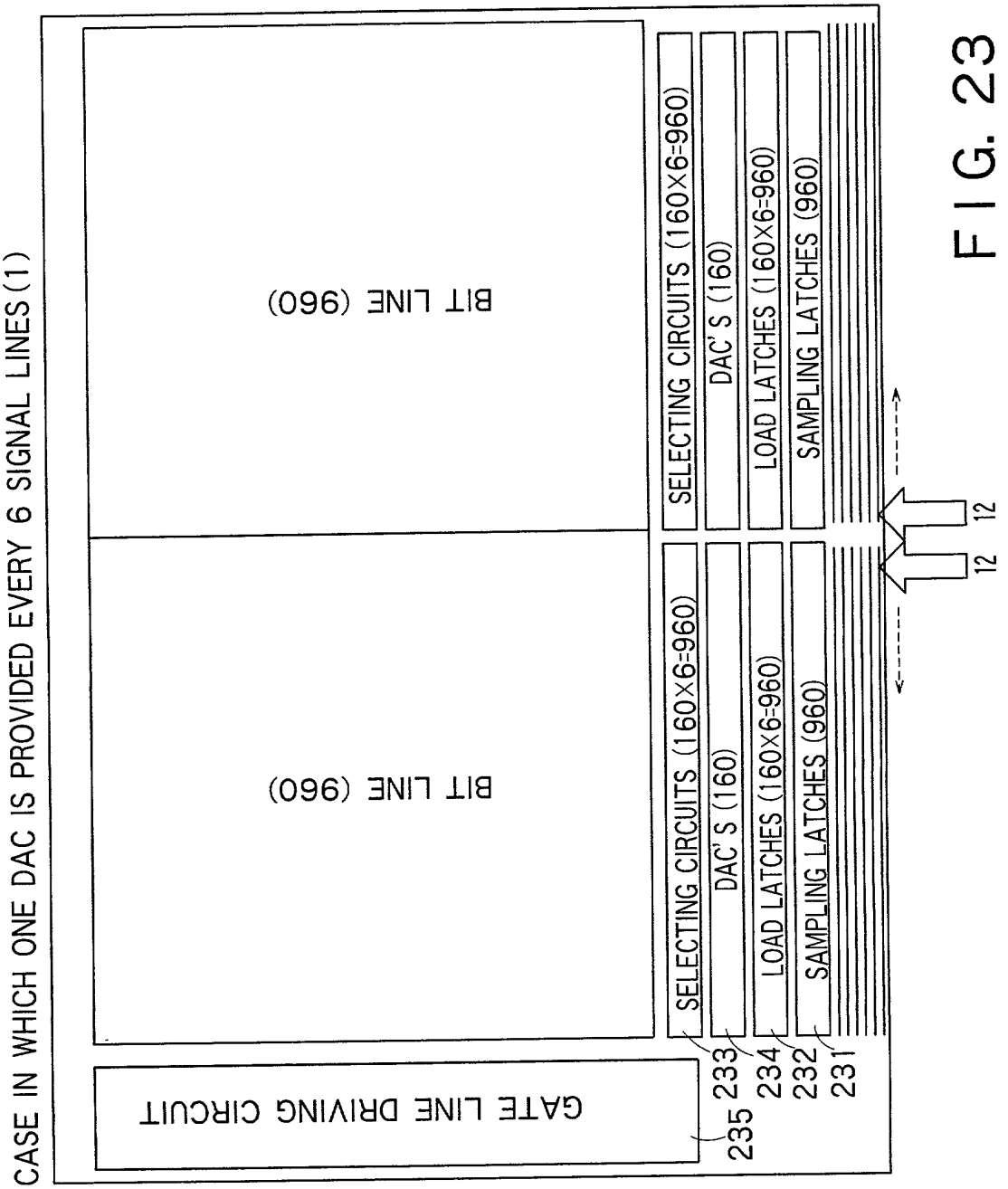
CASE IN WHICH ONE DAC IS PROVIDED EVERY 6 SIGNAL LINES (1)
BIT LINE (960)
BIT LINE (960)
SELECTING CIRCUITS (160×6=960)
DAC'S (160)
LOAD LATCHES (160×6=960)
SAMPLING LATCHES (960)
SELECTING CIRCUITS (160×6=960)
DAC'S (160)
LOAD LATCHES (160×6=960)
SAMPLING LATCHES (960)
GATE LINE DRIVING CIRCUIT
231
232
234
233
235
12
12

FIG. 23

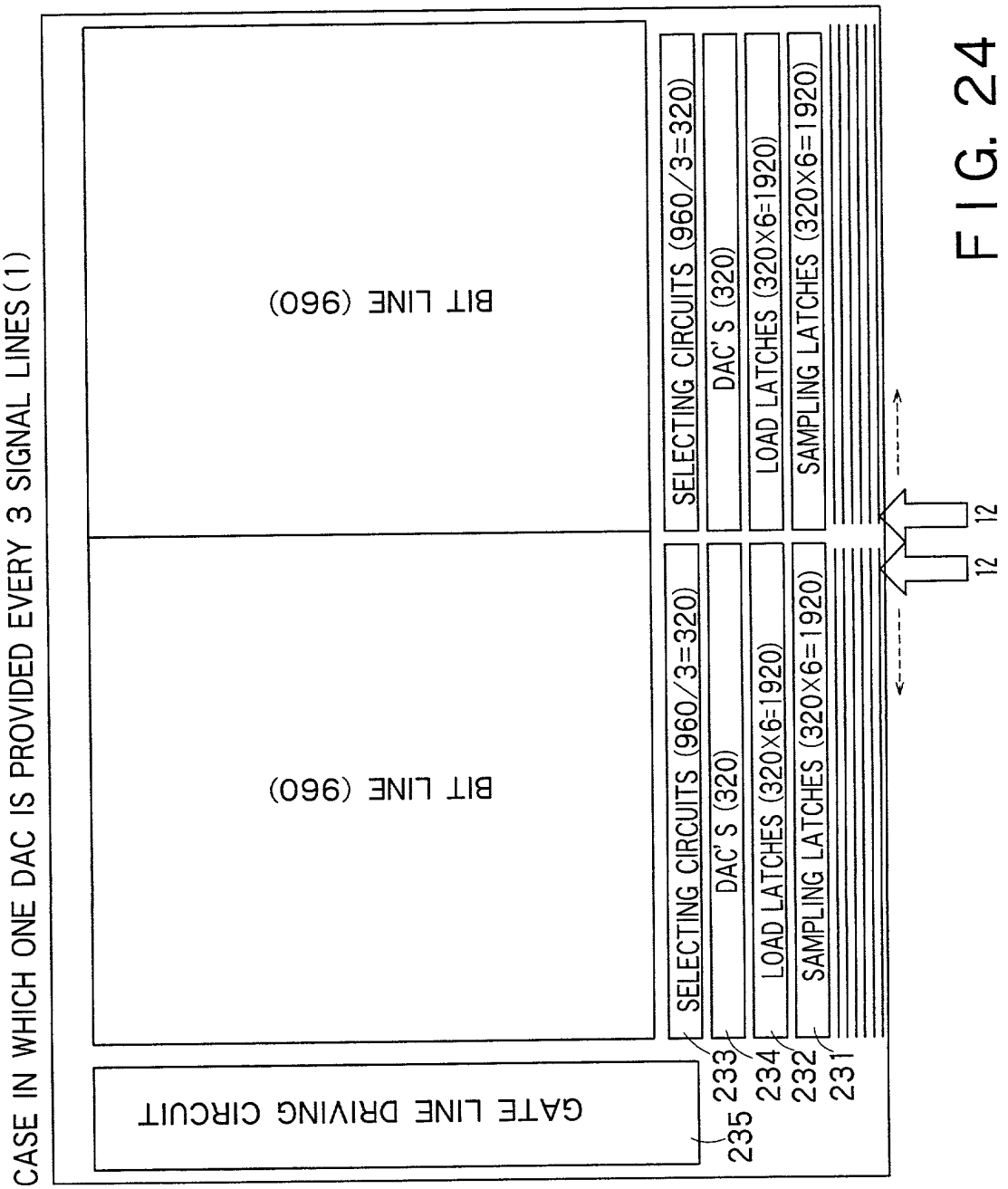
CASE IN WHICH ONE DAC IS PROVIDED EVERY 3 SIGNAL LINES (1)
BIT LINE (960)
BIT LINE (960)
GATE LINE DRIVING CIRCUIT
SELECTING CIRCUITS (960/3=320)
DAC'S (320)
LOAD LATCHES (320×6=1920)
SAMPLING LATCHES (320×6=1920)
SELECTING CIRCUITS (960/3=320)
DAC'S (320)
LOAD LATCHES (320×6=1920)
SAMPLING LATCHES (320×6=1920)
231
232
234
233
235
12
12

FIG. 24

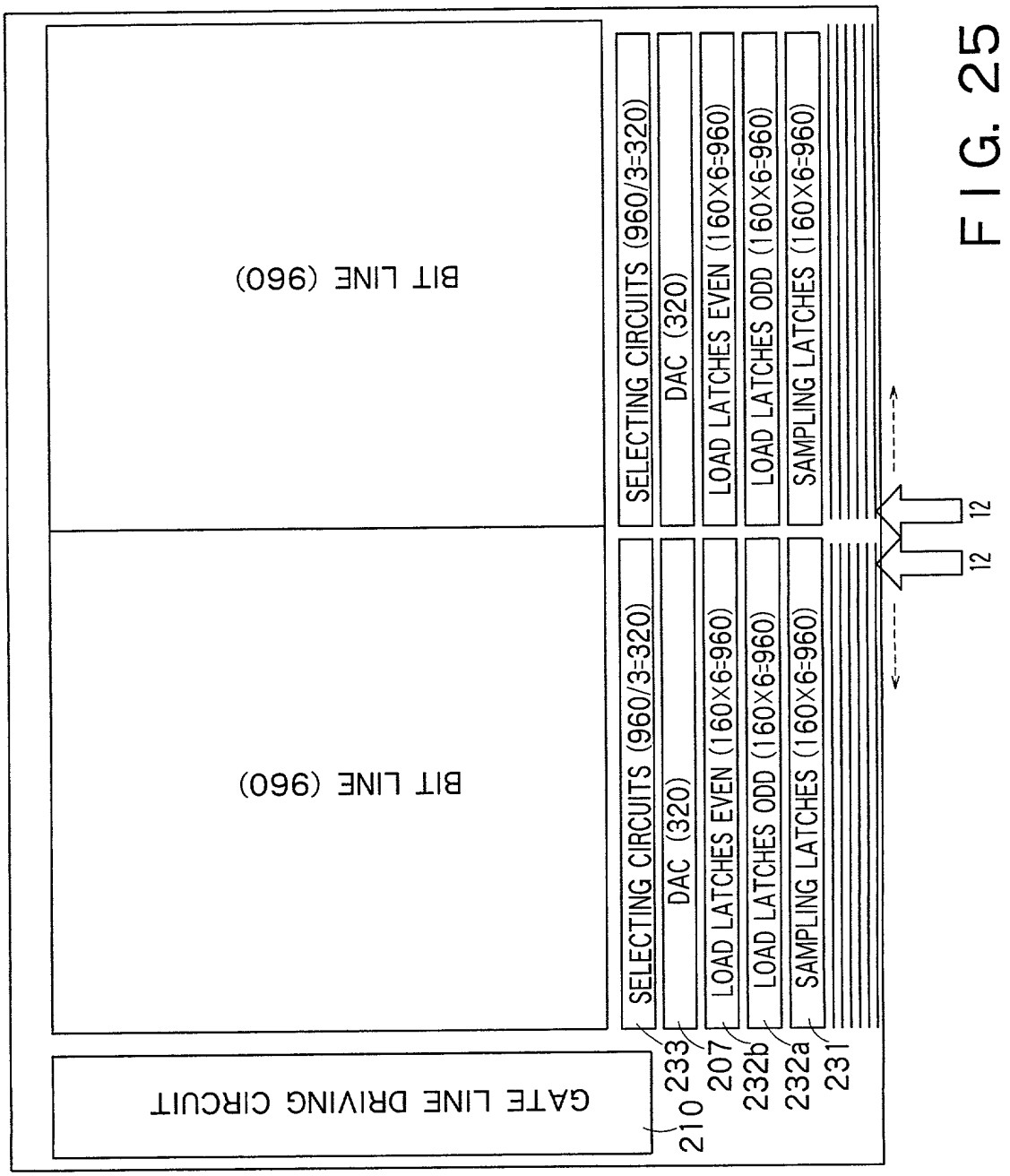
BIT LINE (960)
BIT LINE (960)
SELECTING CIRCUITS (960/3=320)
DAC (320)
LOAD LATCHES EVEN (160X6=960)
LOAD LATCHES ODD (160X6=960)
SAMPLING LATCHES (160X6=960)
SELECTING CIRCUITS (960/3=320)
DAC (320)
LOAD LATCHES EVEN (160X6=960)
LOAD LATCHES ODD (160X6=960)
SAMPLING LATCHES (160X6=960)
12
12
GATE LINE DRIVING CIRCUIT
210
233
207
232b
232a
231

FIG. 25

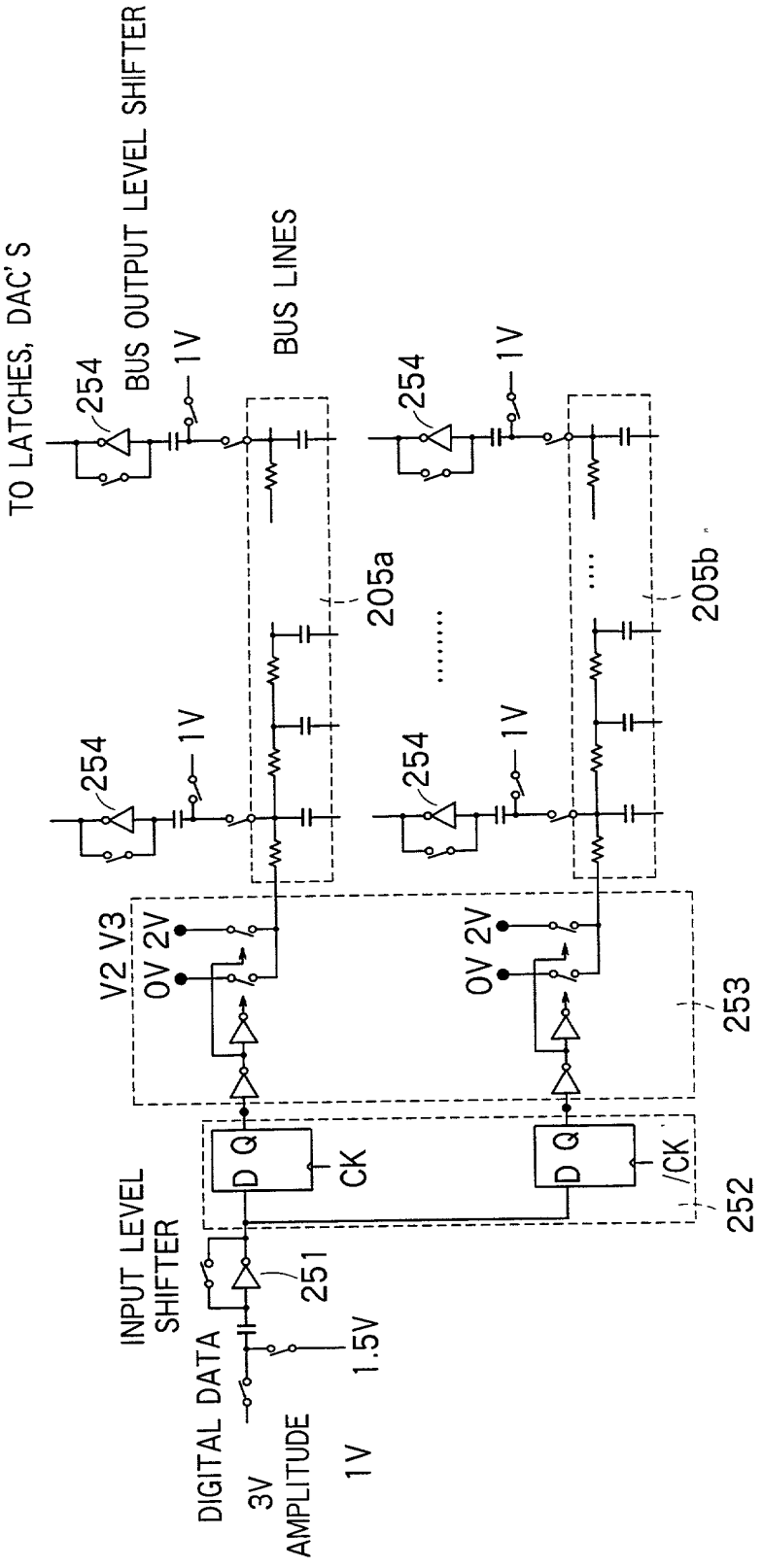
TO LATCHES, DAC'S
BUS OUTPUT LEVEL SHIFTER
BUS LINES
254
1V
205a
205b
V2 V3
0V 2V
253
D Q
CK
/CK
252
INPUT LEVEL SHIFTER
251
DIGITAL DATA
3V AMPLITUDE
1V
1.5V

FIG. 26

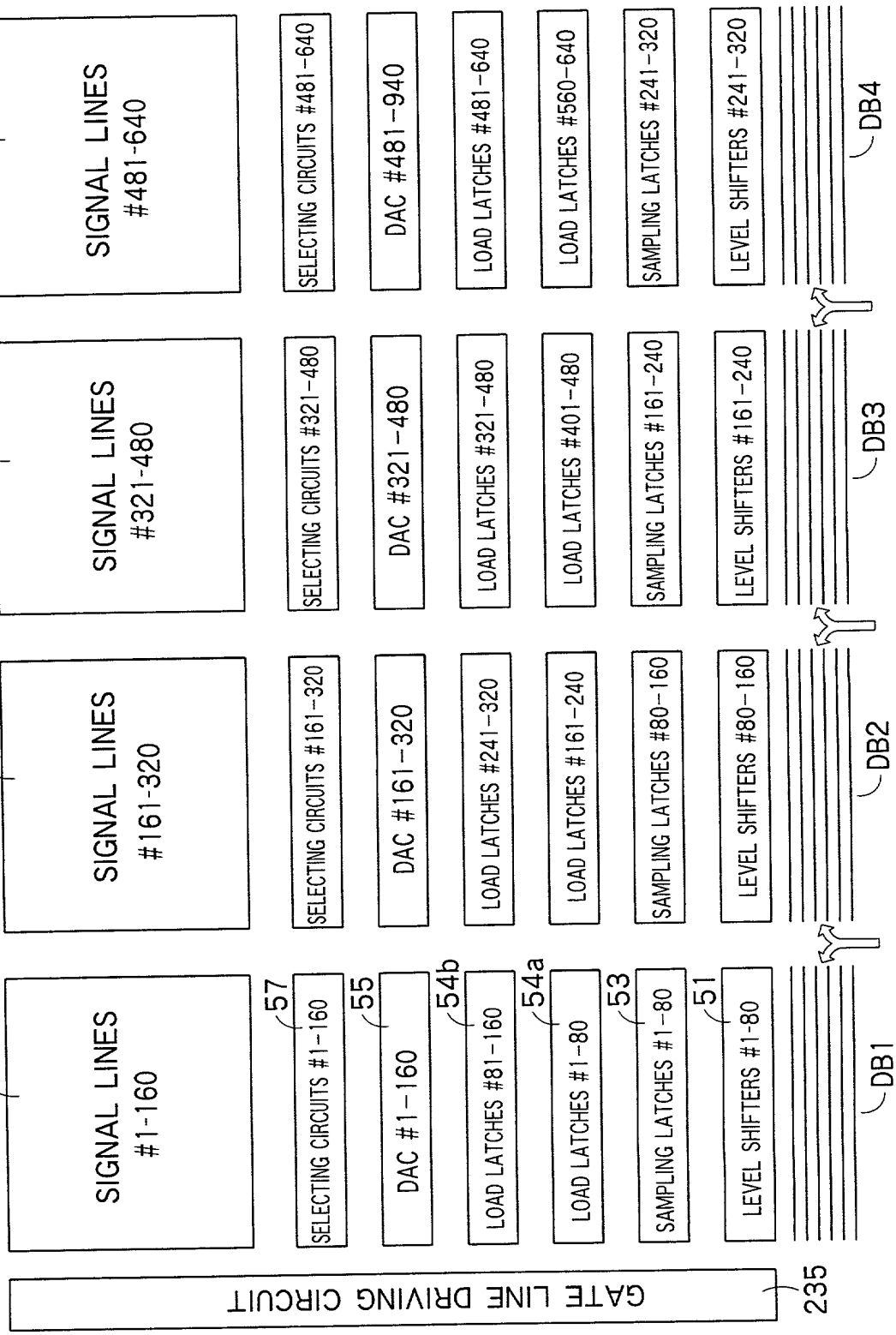
B1
SIGNAL LINES #1-160
B2
SIGNAL LINES #161-320
B3
SIGNAL LINES #321-480
B4
SIGNAL LINES #481-640
57
SELECTING CIRCUITS #1-160
SELECTING CIRCUITS #161-320
SELECTING CIRCUITS #321-480
SELECTING CIRCUITS #481-640
55
DAC #1-160
DAC #161-320
DAC #321-480
DAC #481-940
54b
LOAD LATCHES #81-160
LOAD LATCHES #241-320
LOAD LATCHES #321-480
LOAD LATCHES #481-640
54a
LOAD LATCHES #1-80
LOAD LATCHES #161-240
LOAD LATCHES #401-480
LOAD LATCHES #560-640
53
SAMPLING LATCHES #1-80
SAMPLING LATCHES #80-160
SAMPLING LATCHES #161-240
SAMPLING LATCHES #241-320
51
LEVEL SHIFTERS #1-80
LEVEL SHIFTERS #80-160
LEVEL SHIFTERS #161-240
LEVEL SHIFTERS #241-320
DB1
DB2
DB3
DB4
GATE LINE DRIVING CIRCUIT
235

FIG. 27

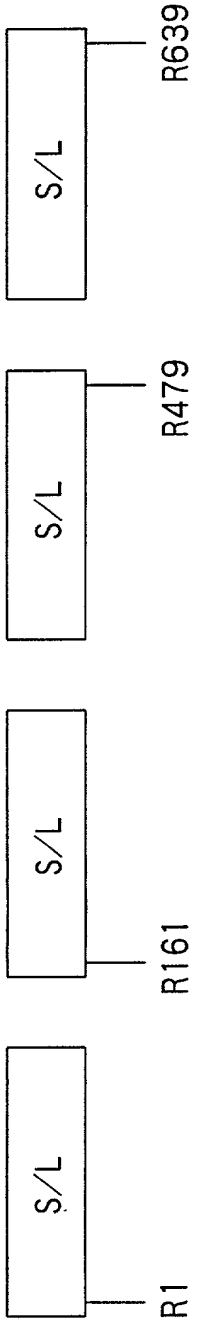

FIG. 28A

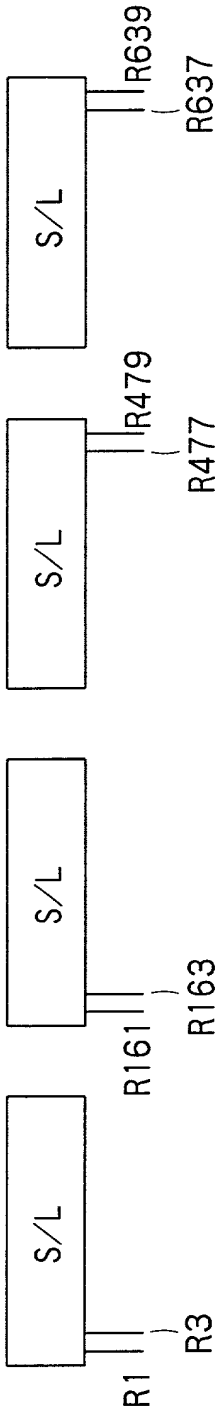

FIG. 28B

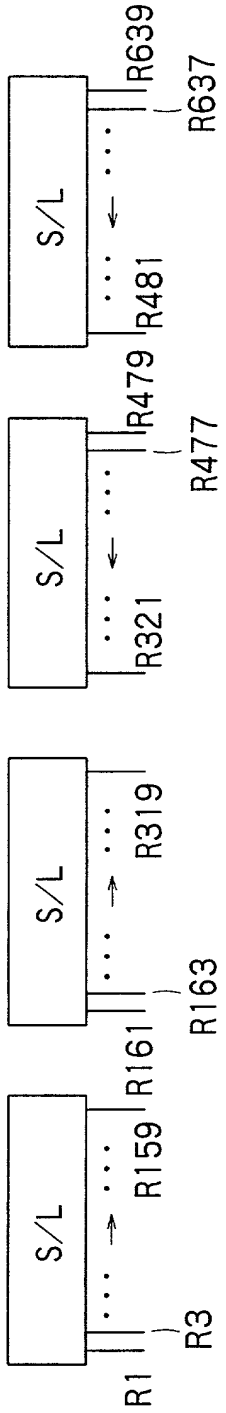

FIG. 28C

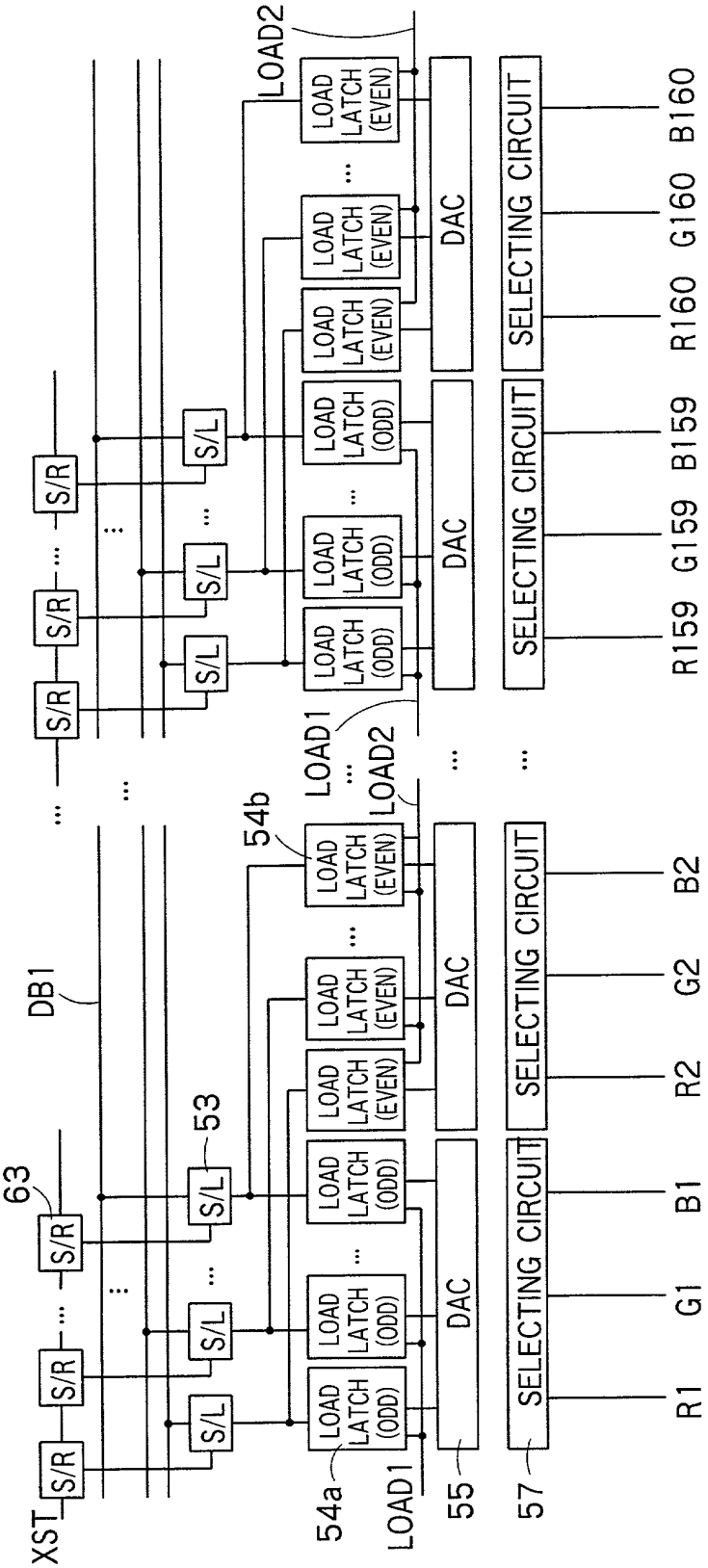
XST
S/R
63
DB1
S/L
53
54a
54b
LOAD1
LOAD2
LOAD LATCH (ODD)
LOAD LATCH (EVEN)
DAC
55
SELECTING CIRCUIT
57
R1
G1
B1
R2
G2
B2
R159
G159
B159
R160
G160
B160

FIG. 29

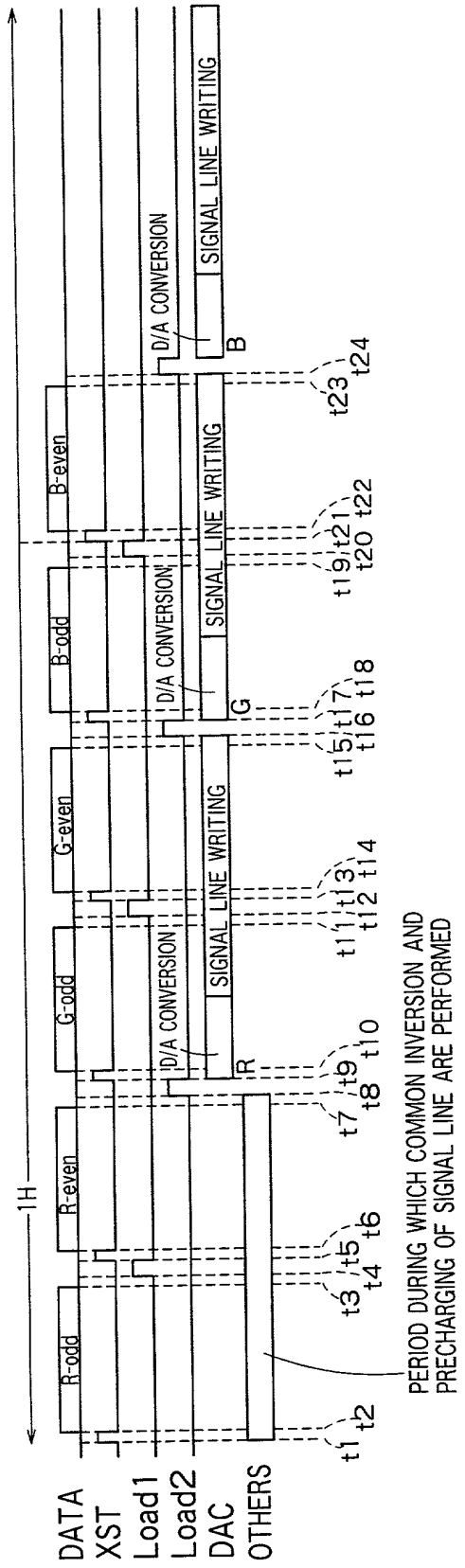
DATA
XST
Load1
Load2
DAC
OTHERS
1H
R-odd
R-even
G-odd
G-even
B-odd
B-even
D/A CONVERSION
SIGNAL LINE WRITING
R
G
B
t1
t2
t3
t4
t5
t6
t7
t8
t9
t10
t11
t12
t13
t14
t15
t16
t17
t18
t19
t20
t21
t22
t23
t24
PERIOD DURING WHICH COMMON INVERSION AND
PRECHARGING OF SIGNAL LINE ARE PERFORMED

FIG. 30

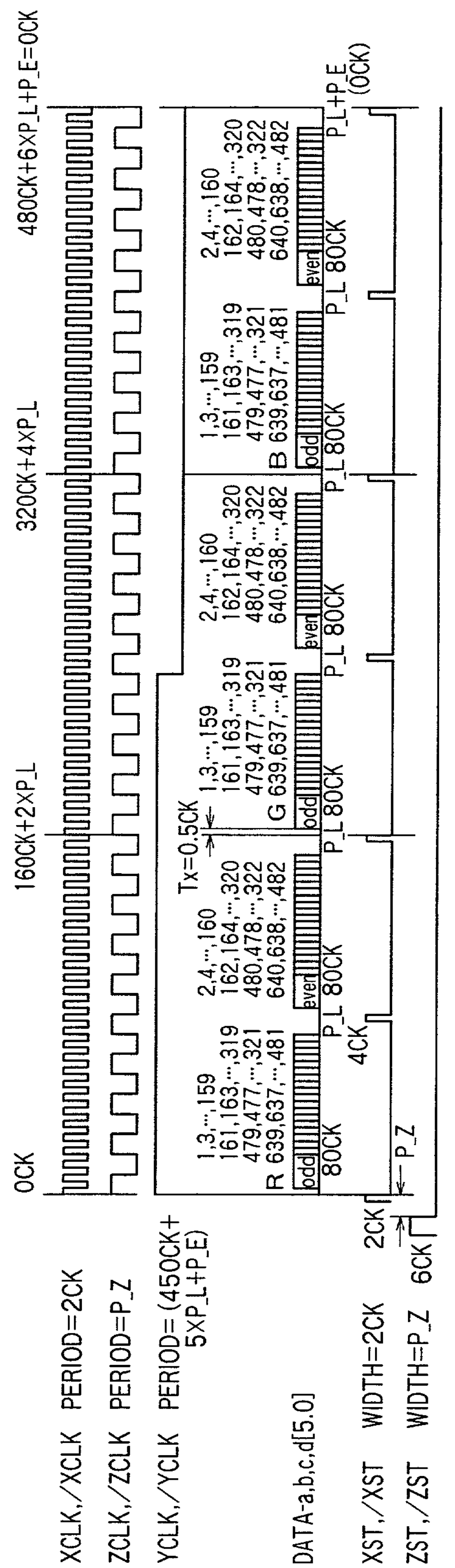
XCLK,/XCLK PERIOD=2CK
ZCLK,/ZCLK PERIOD=P_Z
YCLK,/YCLK PERIOD=(450CK+5XP_L+P_E)
DATA-a,b,c,d[5.0]
XST,/XST WIDTH=2CK
ZST,/ZST WIDTH=P_Z
0CK
160CK+2XP_L
320CK+4XP_L
480CK+6XP_L+P_E=0CK
Tx=0.5CK
R 639,637,…,481
479,477,…,321
161,163,…,319
1,3,…,159
G 639,637,…,481
B 639,637,…,481
2,4,…,160
162,164,…,320
480,478,…,322
640,638,…,482
odd
even
80CK
P_L
4CK
P_Z
2CK
6CK
P_L+P_E
(0CK)

FIG. 31

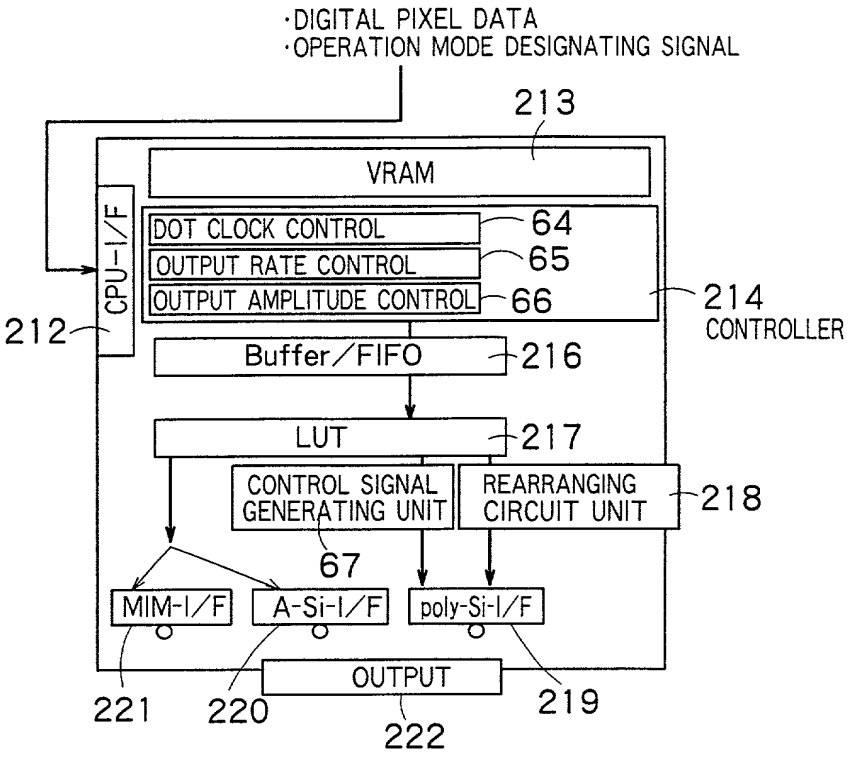
·DIGITAL PIXEL DATA
·OPERATION MODE DESIGNATING SIGNAL
213
VRAM
CPU-I/F
DOT CLOCK CONTROL
64
OUTPUT RATE CONTROL
65
OUTPUT AMPLITUDE CONTROL
66
214
CONTROLLER
212
Buffer/FIFO
216
LUT
217
CONTROL SIGNAL GENERATING UNIT
REARRANGING CIRCUIT UNIT
218
67
MIM-I/F
A-Si-I/F
poly-Si-I/F
OUTPUT
221
220
219
222

FIG. 32

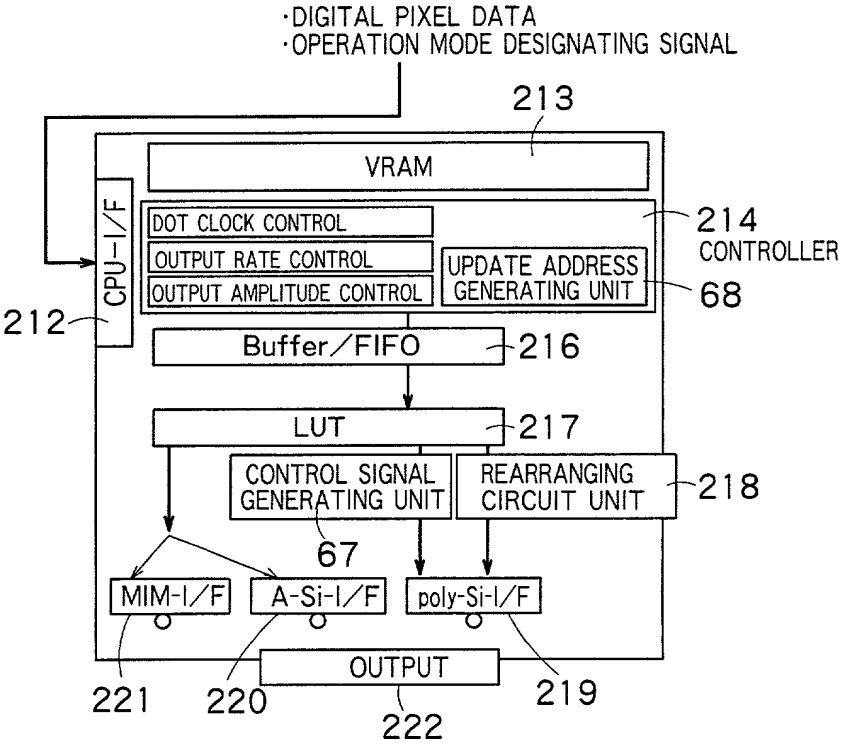
·DIGITAL PIXEL DATA
·OPERATION MODE DESIGNATING SIGNAL
213
VRAM
CPU-I/F
DOT CLOCK CONTROL
OUTPUT RATE CONTROL
OUTPUT AMPLITUDE CONTROL
UPDATE ADDRESS GENERATING UNIT
68
214
CONTROLLER
212
Buffer/FIFO
216
LUT
217
CONTROL SIGNAL GENERATING UNIT
REARRANGING CIRCUIT UNIT
218
67
MIM-I/F
A-Si-I/F
poly-Si-I/F
OUTPUT
221
220
219
222

FIG. 33

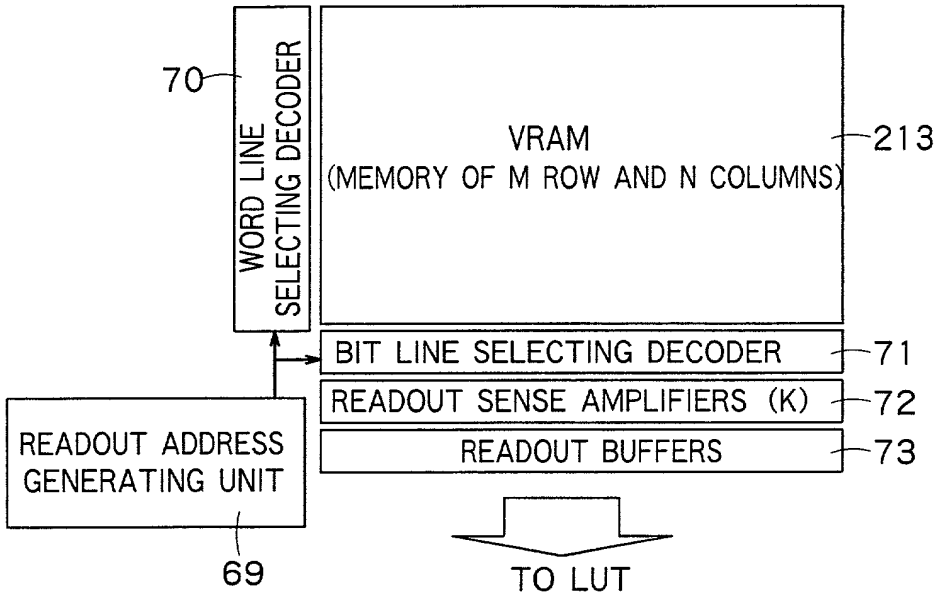
70
WORD LINE SELECTING DECODER
VRAM
(MEMORY OF M ROW AND N COLUMNS)
213
BIT LINE SELECTING DECODER
71
READOUT SENSE AMPLIFIERS (K)
72
READOUT BUFFERS
73
READOUT ADDRESS GENERATING UNIT
69
TO LUT

FIG. 34

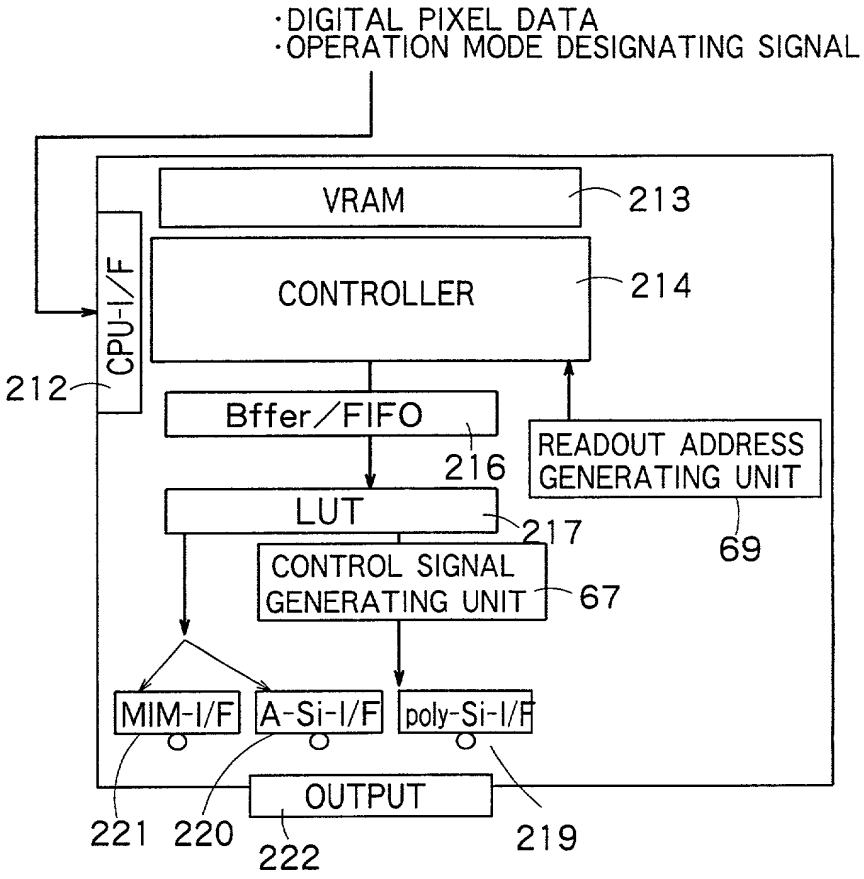
·DIGITAL PIXEL DATA
·OPERATION MODE DESIGNATING SIGNAL
VRAM
213
CONTROLLER
214
CPU-I/F
212
Bffer/FIFO
216
READOUT ADDRESS GENERATING UNIT
69
LUT
217
CONTROL SIGNAL GENERATING UNIT
67
MIM-I/F
A-Si-I/F
poly-Si-I/F
OUTPUT
221
220
222
219

FIG. 35

30 / 30

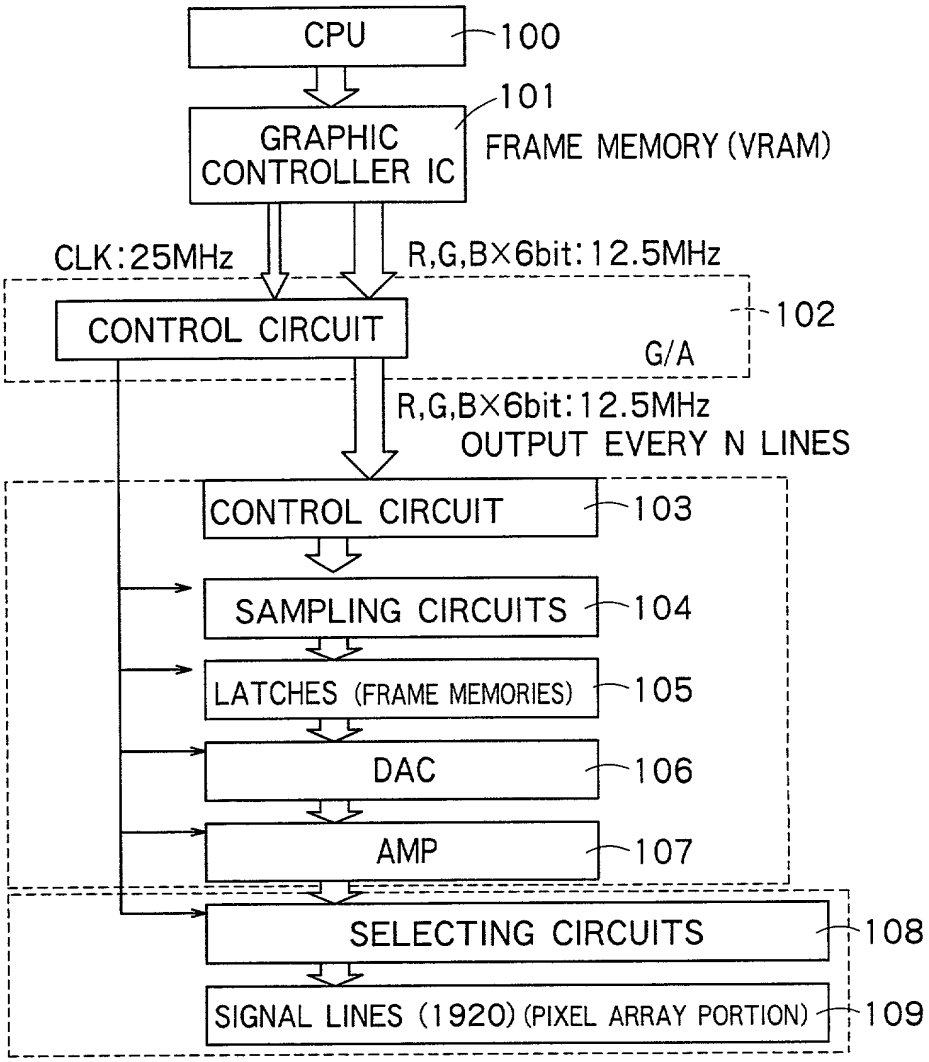
CPU
100
101
GRAPHIC CONTROLLER IC
FRAME MEMORY (VRAM)
CLK:25MHz
R,G,B×6bit:12.5MHz
CONTROL CIRCUIT
102
G/A
R,G,B×6bit:12.5MHz
OUTPUT EVERY N LINES
CONTROL CIRCUIT
103
SAMPLING CIRCUITS
104
LATCHES (FRAME MEMORIES)
105
DAC
106
AMP
107
SELECTING CIRCUITS
108
SIGNAL LINES (1920) (PIXEL ARRAY PORTION)
109

FIG. 36